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Phase Shift APOD and POD Control Technique in Multi-Level Inverters to Mitigate Total Harmonic Distortion

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Abstract: Multi-level inverters are widely employed to generate new energy because of their huge capacity and benefits in sound control performance. One of the critical areas of study for multi-level inverters is control strategy research. In this study, the control strategy for a multi-level inverter—which is frequently employed in HVDC and FACTS systems—is designed. An asymmetrical D.C. voltage source is supplied to create the appropriate output voltage waveform with fewer total harmonic distortions (THDs) at the output voltage and current waveforms. In this work, the pulse width modulation techniques of POD (phase opposition disposition) and APOD (alternative phase opposition disposition) MC PWM are applied to a multi-level inverter to generate the seven-level output voltage waveform. This study presents an enhanced variable carrier frequency APOD control approach that can successfully lower the overall harmonic distortion rate. The design and completion of the phase-shifting POD and APOD control strategies are followed by an analysis and comparison of the THD situation under various switching frequencies and a simulation and verification of the control strategy using MATLAB simulation. The TI DSP-based control approach has been programmed. The APOD technique increases the output voltage's THD to 18.27%, while the output current waveform's THD is reduced to 15.67% by utilizing the APOD PWM technique. Using the POD PWM approach increases the total harmonic distortion (THD) of the voltage waveform by 18.06% and the output current waveform's THD by 15.45%.

Keywords: level-shifted POD; level-shifted APOD; THD; DSP control

MSC: 65T50



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1. Introduction

A multi-level inverter is a power electronic system that uses a low-level D.C. voltage as input to provide the required A.C. voltage output. As a new type of high-power inverter, the multi-level inverter can generate high voltage and reduce harmonics through its circuit topology. Therefore, multi-level voltage source converters often appear in high-power applications [1]. Multi-level voltage source converters synthesize stepped voltage waves from several D.C. capacitive voltages. One of the significant limitations of multi-level converters is the voltage imbalance between different levels. Techniques for balancing voltages between different levels usually include voltage clamping or capacitive charging control [2]. There are many ways to achieve voltage balance in multi-level converters.

The sum of the inverter's output voltage is equal to the output voltage of the M-class inverter. The difference lies in the multi-level inverter's switching mechanism and the input voltage's source [3].

Traditional two and three-level inverters have many limitations when dealing with high voltage and power conversion. With a higher capacity and reduced output voltage harmonic distortion, the converter is connected in series with the transformer. This is assumed to be the primary harmonic elimination method of the multi-level inverter; the improvement of power quality is also crucial to researching and comparing different topologies of pulse width modulation [4]. The international community currently relies heavily on non-renewable energy, but after the recent oil crisis, increasing the use of renewable energy has become a top priority for many countries due to its numerous benefits, including minimal environmental impact. Unlike conventional generators, renewable energy needs less maintenance and has a significant economic effect [5]. Today, the electronic world is a global society. In the future, industrial society will be led by two technologies: highly automated computers and power electronics. Multi-level inverters are commonly used in various industries. Applications include hybrid active harmonic filters, reactive power compensation, traction, electric vehicles, single-phase and three-phase induction motor speed control, and more [6]. They are also used in the renewable energy sector. In recent years, electrical engineering researchers have paid attention to multi-level inverters in many industrial applications in terms of quality and reliable power [7]. To improve the efficiency of solar photovoltaic energy conversion systems, a multi-level inverter was developed as a viable alternative to traditional straight-beam transducer renewable energy systems [8].

The multi-level inverter (MLI) has become a fascinating and powerful DC-AC converter among various inverter schemes. In many power electronics applications, the MLI has been a significant research area in power electronics in recent years because of its advantages, such as low switching loss, strong voltage operation ability, high efficiency, low voltage, and slight electromagnetic interference. A novel topology for the multi-level inverter based on the series connection of basic modules has been developed. The suggested topology is utilized for symmetrical and asymmetric source systems, which can be used for fuel cell and photovoltaic systems [9]. A new multi-level inverter topology employing the concept of half-bridge modules is suggested in this paper. It requires a lower number of DC sources and power components. The inverter is controlled using a fundamental frequency-switching scheme [10]. The proposed control strategy simplifies the design of the control system, reduces the computational burden, and can be easily extended to MMC with any S.M. number [11]. In this study, equations for combining different pulse width modulation (PWM) techniques to use the controllability advantage of the multi-carrier method are introduced in asymmetric topologies [12]. The proposed study suggests the application of a whale optimization algorithm (WOA) based on a fractional-order proportional-integral controller (FOPIC) for unified power quality conditioner (UPQC) and STATCOM tools; furthermore, since the output is similar to sinusoidal waves, it has the benefits of good power efficiency, low harmonic distortion, and low EMI [13].

The lower-order harmonics in the inverters and modulation techniques highly affect the performance and efficiency of the system and are suitable for PWM, which is used to control and mitigate these effects. Currently, most inverters seem to be quasi-square wave inverters with a lot of distortion. Researchers are working hard to create and commercialize effective, distortion-free inverters [14]. Low cost, reduced switching complexity, and efficient filtering are also priorities in inverter architecture. While single-pole and bipolar inverters are well-known, much room remains for improvement [15].

Table 1 provides a descriptive and critical table summary of the literature review showing the research gaps.

Table 1. Descriptive and critical table summary of the literature review.

Ref(s)	PWM Technology	Applications	Key Findings	Research Gaps/Opportunities
[16]	SPWM and Various PWM Techniques	General Inverter Applications	Discussed effective filter design principles and observed various PWM techniques.	Future work could explore optimization of filter designs for specific applications to further reduce THD
[17,18]	SHEPWM, Optimized PWM, SVPWM	Multi-level Inverters	Presented several important digital PWM technologies simplifying PWM generation.	Development of more efficient algorithms for PWM generation to reduce computational complexity.
[19]	Sinusoidal and Square PWM	Asymmetrical Multi-level Structures	Lower THD at output voltage with fewer components in asymmetrical arrangements.	Investigate the scalability of asymmetrical designs in higher-power applications.
[20]	Carrier-based PWM (PDPWM, PODPWM, APODPWM)	H-Bridge Multi-level Inverters	Compared different carrier-based PWM strategies for THD reduction.	Comparative studies on the efficiency and performance of these PWM strategies in real-world applications.
[21]	Duty Cycle PWM	Voltage Regulation	Utilized the duty cycle for inverter output voltage regulation.	Deep dive into adaptive duty cycle strategies for dynamic load conditions.
[22]	Bipolar SPWM	Low-power Inverters	High performance with bipolar PWM when sinusoidal signal level is higher than the triangle signal level.	Explore the limitations and performance in high-power scenarios.
[23]	Multi-level Inverter	High-power Applications	Improved power quality with increased output voltage levels.	Addressing the increase in component count and switching losses with higher levels.
[24]	Filter Design	Signal Processing	Emphasized the importance of filters in achieving pure sine wave outputs.	Innovation in filter design to further reduce THD in inverter outputs.
[25]	Inverter Switching and Voltage Levels	Polarity and Level Generation	Detailed the operation of IGBT switches in generating output voltage levels.	Examination of alternative switching materials and technologies for efficiency improvements.
[26]	Simulation and Control	Inverter Design	Utilized MATLAB for simulation and control of multi-level inverters.	Advancements in simulation tools for more accurate prediction of inverter behavior under diverse conditions.

The main contributions of the paper are as follows:

- A cascaded H-bridge multi-level inverter performs much better than the traditional two-level inverter because it reduces the total harmonic distortion (THD), the switch rating, and the electromagnetic performance.
- By comparing the traditional two-level inverter with the cascade H-bridge multi-level inverter, it can be found that the THD decreases with the increase in the multi-level inverter topology level. Signal power quality is also improving.
- The results show that the power quality improves with the increase in the frequency modulation ratio. The switching loss of the inverter increases with the addition of the switching frequency.
- The control uses sinusoidal pulse width modulation (SPWM) to minimize the THD by using P.D. and POD technologies. This design minimizes the output voltage, THD, or harmonic value while reducing switching losses.
- Single-pole PWM inverters have been found to be more efficient than bipolar PWM inverters because there are three levels of single-pole inverters compared to two levels

of bipolar inverters. The larger the output level, the simpler the filter's total harmonic distortion (THD).

- By comparing unipolar and bipolar systems, it can be observed that the THD decreases as the level of the multi-level inverter topology increases. The signal power efficiency is also improving. It also has the disadvantage of increasing the complexity of switching.

The second section of this paper introduces the latest research on sinusoidal pulse width modulation (SPWM). The third section discusses the MATLAB simulation results of different multi-level technologies for seven-level inverters, including POD and APOD, to lower the switching complexity circuit of seven-level inverters. The fourth section gives the simulation discussion and results. The fifth section concludes the paper.

2. Related Works

Inverters with sinusoidal pulse width modulation (SPWM), effective filter design principles, and various PWM techniques are discussed and observed [16]. The literature review and multiple recommendations made by the authors in this field are considered.

2.1. Pulse Width Modulation (PWM) Technology

The most popular switching technology is pulse width modulation (PWM), which has been implemented in most VSI. The simulation technology is based on comparing carrier and pure sinusoidal modulation signals. Its digital version uses the conventional sampling method. It greatly simplifies the generation of PWM and has become the driving force for developing several important digital PWM technologies. Currently, several popular PWM schemes include Selective Harmonic Elimination PWM (SHEPWM), Optimized PWM, and the more recent Space Vector PWM (SVPWM) [17,18]. The modulation techniques used in the switching schemes of the designed multi-level inverters include sinusoidal pulse width modulation and adjusted square pulse width modulation. It is found that the proposed multi-level structure will produce a lower total harmonic distortion at the output voltage. Additionally, the asymmetrical arrangement produces the same output voltage levels with fewer components [19]. This paper presents a 15-stage cascade control strategy of the H-bridge multi-level inverter SPWM. This approach compares a sine wave to a triangular carrier wave with a different phase relationship. This paper examines the carrier-based phase dispositions PDPWM, PODPWM, and APODPWM [20]. Given this fact, there are three basic types of PWM methods: natural sampling PWM, conventional sampling PWM, and direct PWM. For each carrier signal, the reference signal is constantly compared. If the reference is greater than the carrier signal, rather than if the reference is less than the carrier signal, the active device corresponding to the carrier is turned on, and the active device corresponding to the carrier is turned off. The amplitude modulation index m_a , more often than m_f , is defined in the multi-level inverter.

$$m_a = \frac{A_m}{(m-1) \cdot A_c} \quad (1)$$

$$m_f = \frac{f_c}{f_m} \quad (2)$$

Researchers have proposed a carrier-based multi-level sinusoidal triangle PWM scheme to control multi-level diode-clamped inverters with a static reactive power compensator or motor drive. Others also applied the space vector PWM principle to multi-level inverters, which is regulated using the third PWM process. Selective detuning is possible with multi-level diode-clamped converters. There is a significant difference between PWM at two levels and PWM at multiple levels. In two-level PWM, when the modulation index is less than one, the switching frequency always equals the carrier frequency. In multi-level PWM, the switching frequency can be less than or greater than the carrier frequency, and it is a function of the shift angle between the carrier group and the modulation waveform. The number of switches for a particular active device is minimized by selecting a phase

displacement angle, m_a and m_f , which can reduce the switching loss by up to 35% and significantly improve the inverter's efficiency.

2.2. Duty Cycle of PWM Technology

The PWM scheme uses the service cycle to regulate the inverter's output voltage [21]. The service cycle is expressed as a percentage of the total time. The duration of the switch's operation is "on time," and it is regulated by the duty cycle.

$$D = \frac{T}{P} \times 100\% \quad (3)$$

Here, the duty ratio includes the following:

T is how long it is going to continue to run;

P is the time period.

2.3. PWM Dead Time

While keeping a PWM controller from puncturing is important, blank time is incorporated into the switch to guarantee seamless functioning. The bridge's switches must be turned on properly to provide the intended output. The output voltage varies when two switches on a single arm conduct electricity simultaneously. Because of this, researchers usually incorporate a brief dead time before utilizing PWM approaches.

2.4. Modulation Index

The modulation index is the ratio of the control signal's peak amplitude to the carrier signal.

$$M = \frac{V(p)}{V(c)} \quad (4)$$

where M is the modulation index, $V(p)$ is the amplitude of the control signal, and $V(c)$ is the amplitude of the carrier wave.

2.5. Sinusoidal Pulse Width Modulation (SPWM)

The control signal in SPWM is sinusoidal. Unipolar and bipolar PWM are the two types of sine PWM. These techniques contrast the reference signal, a sinusoidal signal, with the carrier signal, a triangle signal. In contrast, the comparator block is employed. It generates the gate signal. The control signal determines the frequency of the output voltage. The amplitude of the changed signal is measured to keep track of it.

2.5.1. Bipolar Sinusoidal Pulse Width Modulation

The low-power inverter employs the bipolar PWM method. In bipolar PWM technology, a comparator compares the modulating signal (sinusoidal signal) with the carrier signal (triangular signal). Performance will be extremely high when the sinusoidal signal level is higher than the triangle signal level and vice versa [22]. Figure 1 shows the bipolar pulse width modulation (PWM).

2.5.2. Multi-Level Inverter

Multi-level inverters used to produce a low-distortion sine wave. They are used in applications that require a lot of electricity [23]. The waveform will appear to follow the sine wave as the output voltage level rises. As the amount is raised, the inverter's power quality also increases. It also has some disadvantages. The number of components and switching losses increases as the amount rises. It has gate circuits as well.

The gate drive is a power amplifier that uses the controller I.C.'s low power input to produce high-current gate drives for power switches (MOSFETs, IGBTs, and so on). In certain situations, the PWM controller does not have enough output current to open and close the drive power supply's capacitance. Gate drivers are often made up of transistors

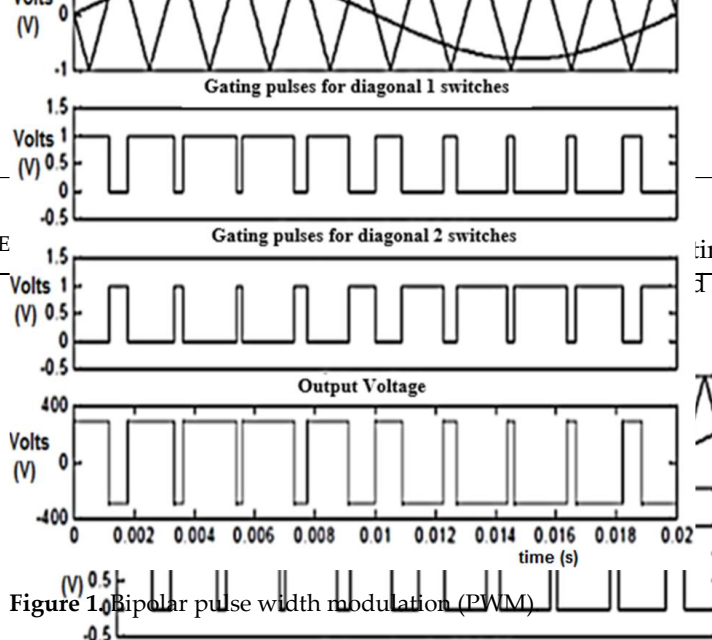


Figure 1. Bipolar pulse width modulation (PWM).

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2.5.2.1. Multi-Level Inverter powered by two H-bridge motors (I.C.) It performs the role of a current amplifier. It receives a low-current control signal at the input and drives the power switch with a high-current drive signal. The amplified current signal powers the motor. The pin diagram of the L293D I.C. is shown in Figure 2.

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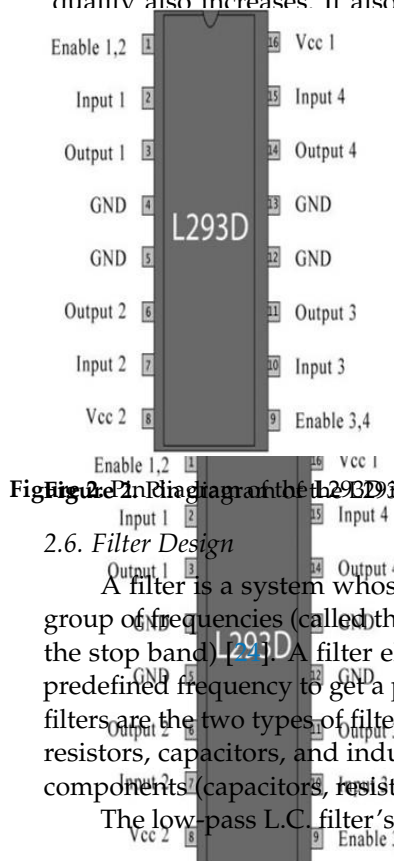


Figure 2. Pin diagram of the L293D integrated circuit.

2.6. Filter Design

A filter is a system whose purpose is to attenuate the signal slightly in a particular group of frequencies (called the passband) and block the signal in a different group (called the stop band) [24]. A filter eliminates any additional frequency components above the predefined frequency to get a pure sine wave (cut-off frequency). Passive filters and active filters are the two types of filters. Passive filters consist only of passive components such as resistors, capacitors, and inductors. Integrated circuits, op-amps, transistors, or passive components (capacitors, resistors, and inductors) are combined in active filters.

The low-pass L.C. filter's transfer function is as follows.

Figure 2. Pin diagram of the L293D integrated circuit.

$$H(s) = \frac{1}{s^2 + \frac{1}{LC}} \tag{5}$$

The cut-off frequency can be obtained in a few different ways.

$$\omega_c = \frac{1}{\sqrt{LC}} \tag{6}$$

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{7}$$

The low and high harmonics are removed by setting the cut-off frequency as close to the 60 Hz fundamental frequency as possible.

2.7. Inverter Switching and Voltage Levels
Level and Polarity Generation

The switching table for the eight IGBTs used in the topology is included in this section [25]. This topology is made up of separate parts for generating the level and polarity. The level of the topology and polarity generation sections are shown in Figure 3.

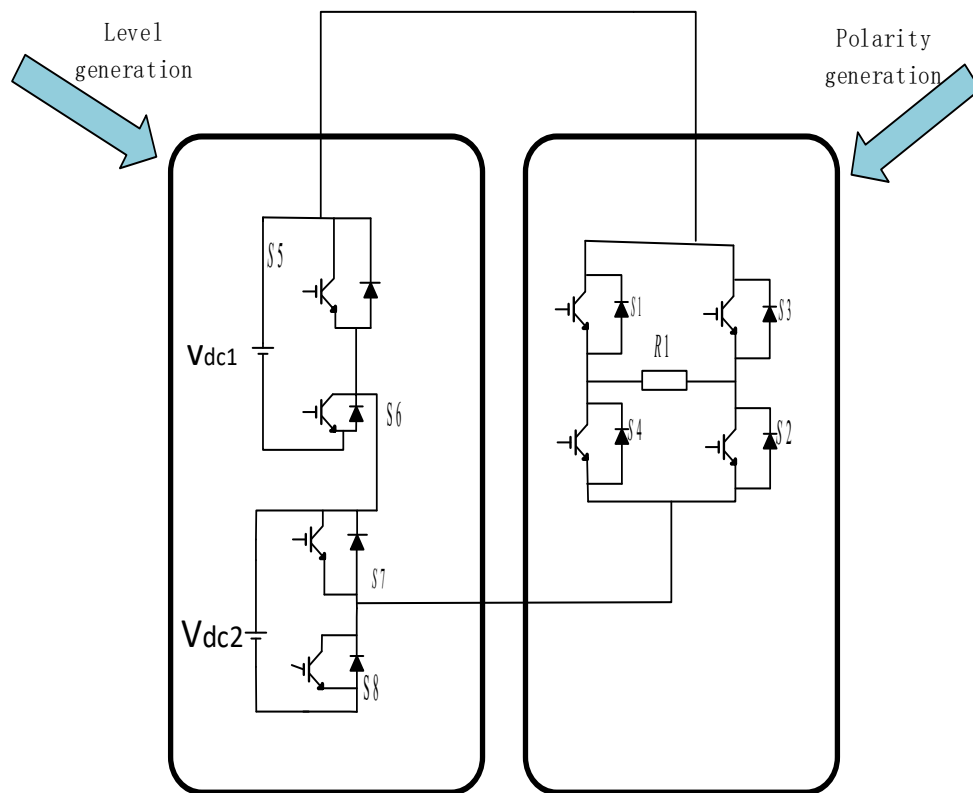


Figure 3: Level and polarity generation.

Switches S1, S2, S3, and S4 are responsible for polarity generation, while switches S5, S6, S7, and S8 are responsible for output voltage levels. Since both Vdc1 and Vdc2 have different voltages, the topology is asymmetric.

Level	S1	S2	S3	S4	S5	S6	S7	S8	Output
0	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	0Vdc
1	ON	ON	OFF	OFF	OFF	ON	ON	OFF	+Vdc
2	ON	ON	OFF	OFF	ON	OFF	OFF	ON	+2Vdc
3	ON	ON	OFF	OFF	ON	ON	OFF	ON	+3Vdc

Table 1 depicts the flipping of the topology's eight switches. Table 2 shows that S1 and S2 are ON during the positive half cycle, while S3 and S4 add to the voltage level during the negative half cycle. The circuit's various operating levels are listed below.

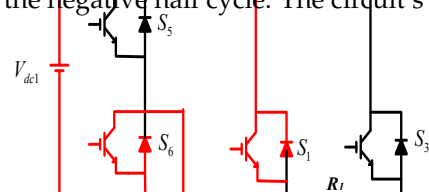


Figure 5. Level 2 of operation.

Table 3. Zero-cycle operation of CHB MLI.

Level	S1	S2	S3	S4	S5	S6	S7	S8	Output
0 V	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	0

Level 3: Switches 1, 2, 6, and 8 are activated in this mode. $(V_{dc1} + V_{dc2})$ is the voltage that appears through the load. Figure 6 depicts the current course.

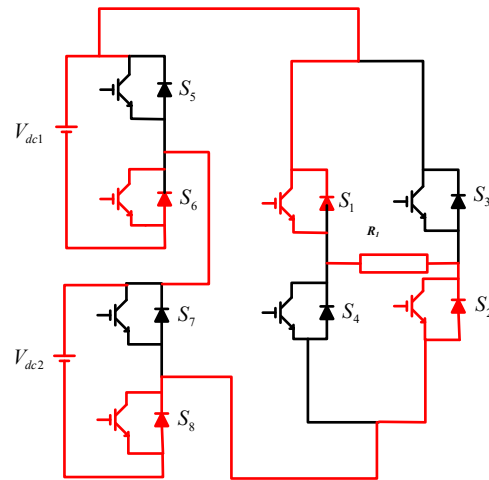


Figure 6. Level 3 of operation.

The zero-cycle operation of CHB MLI values are given in Table 3. At the same time, the negative cycle operation of CHB MLI is shown in Table 4. Zero-cycle operation of CHB MLI are shown in Figure 7.

Table 3. Zero-cycle operation of CHB MLI.

Level	S1	S2	S3	S4	S5	S6	S7	S8	Output
0 V	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	0

Table 4. Negative cycle operation of CHB MLI.

Level	S1	S2	S3	S4	S5	S6	S7	S8	Output
4	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	0
5	OFF	OFF	ON	ON	OFF	ON	ON	OFF	$-V_{dc}$
6	OFF	OFF	ON	ON	ON	OFF	OFF	ON	$-2V_{dc}$
7	OFF	OFF	ON	ON	OFF	ON	OFF	ON	$-3V_{dc}$

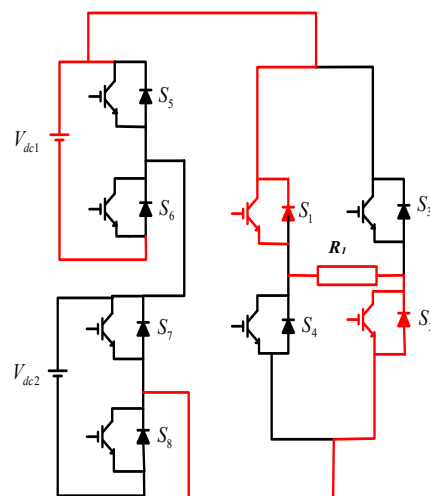


Figure 7. Operation of zero level.

Level 5: Switches 3, 4, 6, and 7 are activated in this mode. The voltage across the load is $-V_{dc1}$, and the load current direction is shown in Figure 8.

Table 4. Negative cycle operation of CHB MLI.

Level	S1	S2	S3	S4	S5	S6	S7	S8	Output
4	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	0
5	OFF	OFF	ON	ON	OFF	ON	ON	OFF	$-V_{dc}$
6	OFF	OFF	ON	ON	ON	OFF	OFF	ON	$-2V_{dc}$
7	OFF	OFF	ON	ON	OFF	ON	OFF	ON	$-3V_{dc}$

1	OFF	OFF	ON	ON	OFF	ON	ON	OFF	-Vdc
5	OFF	OFF	ON	ON	OFF	ON	ON	OFF	-2Vdc
6	OFF	OFF	ON	ON	ON	OFF	OFF	ON	-3Vdc
7	OFF	OFF	ON	ON	OFF	ON	OFF	ON	-3Vdc

Level 5: Switches 3, 4, 6, and 7 are activated in this mode. The voltage across the load is $-V_{dc1}$, and the load current direction is shown in Figure 8.

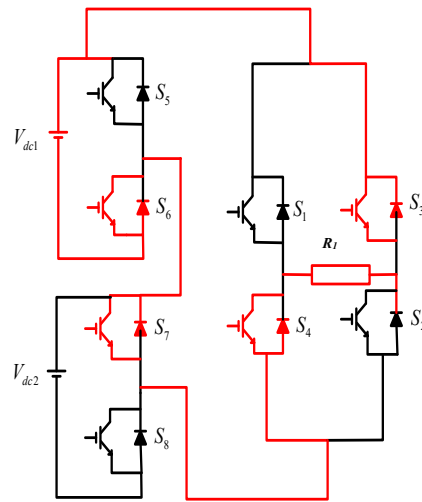


Figure 8. Level of operation 5.

Level 6: Switches 3, 4, 5, and 8 are activated in this mode. The voltage across the load is $-V_{dc2}$, and the load current direction is shown in Figure 9.

Level 7: Switches 3, 4, 6, and 8 are activated in this mode. $-(V_{dc1} + V_{dc2})$ is the voltage that occurs through the load. Figure 10 depicts the current direction.

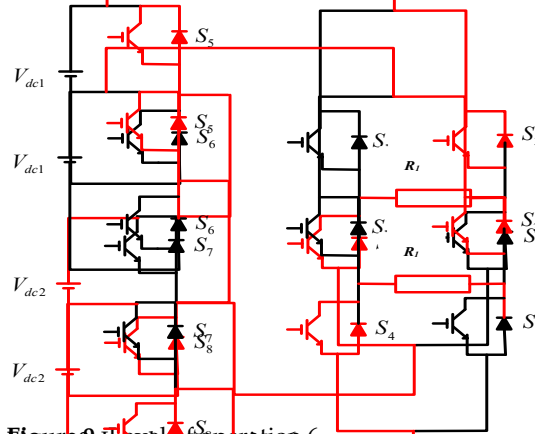


Figure 9. Level of operation 6.

Level 7: Switches 3, 4, 6, and 8 are activated in this mode. $-(V_{dc1} + V_{dc2})$ is the voltage that occurs through the load. Figure 10 depicts the current direction.

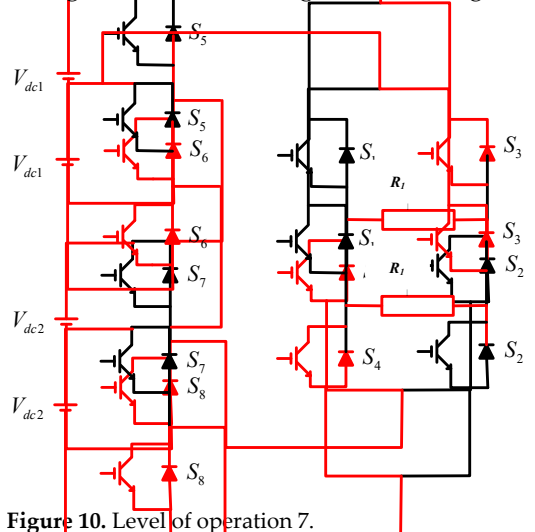


Figure 10. Level of operation 7.

Figure 10. Level of operation 7. Sinusoidal Pulse Width Modulation (SPWM) for Multi-Level Inverter (MLI)

Figure 10. Level of operation 7.

The traditional SPWM modulation technology generates PWM waveforms by comparing triangular carrier waves with sinusoidal modulation waves, while the multi-carrier SPWM modulation technology is based on multi-carrier sinusoidal pulse width modulation [27]. The principle of multi-carrier SPWM modulation technology is to use multiple triangular carrier signals and the same sinusoidal reference signals to generate switching

3. Sinusoidal Pulse Width Modulation (SPWM) for Multi-Level Inverter (MLI)

The traditional SPWM modulation technology generates PWM waveforms by comparing triangular carrier waves with sinusoidal modulation waves, while the multi-carrier SPWM modulation technology is based on multi-carrier sinusoidal pulse width modulation [27]. The principle of multi-carrier SPWM modulation technology is to use multiple triangular carrier signals and the same sinusoidal reference signals to generate switching signals by comparing them. The multi-carrier SPWM technology is one of the most common modulation methods for multi-level inverters. It is a direct extension of the two-stage SPWM technology used in multi-level inverters. There are two kinds of standard multi-carrier SPWM modulation techniques: SPWM based on carrier vertical phase shift and SPWM based on carrier horizontal phase shift. The modulation strategy of POD and APOD belongs to the carrier vertical phase shifting SPWM modulation strategy. Its basic principle is as follows: if the output voltage level of the inverter is n , $n - 1$ triangular carriers with the same frequency and phase are needed. These $N - 1$ carriers are placed side by side to form a carrier group, and the horizontal center line of the group is taken as the actual reference line; the carrier groups are symmetrically distributed below the reference zero line and modulated by the same sinusoidal modulation wave to obtain the corresponding switching pulse control signal.

- POD (phase opposition disposition)

The carrier signals above and below the reference/zero line are in phase. However, they become 180 degrees out of phase below and above the zero line. At the output side of the CHB multi-level inverter, the necessary output voltage waveform is obtained using the POD multi-carrier PWM technique [28].

- APOD (alternate phase opposition disposition)

Any carrier wave shape in APOD modulation is 180 degrees out of phase with its adjacent carrier. Since the APOD and POD systems are the same with three-level inverters, a seven-level inverter addresses the APOD system [29].

- Harmonic analysis of APOD and POD modulation strategies

According to the theory of bilateral Fourier transform, the harmonic expression of the output waveform of any PWM modulation technology based on carrier wave can be expressed as follows:

$$z = F(x, y) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{n0} \cos(ny) + B_{n0} \sin(ny)] + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} [A_{mn} \cos(mx + ny) + B_{mn} \sin(mx + ny)] \quad (8)$$

where, $y = \omega_0 t$, $x = \omega_c t$, $\omega_0 t$ is the base frequency, ω_c is the carrier frequency, and the factor A_{mn} is $A_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} F(x, y) \cos(mx + ny) dx dy$.

Factor B is as follows:

$$B_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} F(x, y) \sin(mx + ny) dx dy$$

Because $y = \omega_0 t$, $x = \omega_c t$, the harmonic form of the voltage contained in formula n can be expressed as $m\omega_c t + n\omega_0 t$, and there are three cases:

1. When $m = 0$, $n \neq 0$, $n\omega_0$ is a fundamental or harmonic wave.
2. When $m = 0$, $n \neq 0$, $m\omega_c$ is the carrier's harmonic and the carrier's multiplier.
3. When $m = 0$, $n \neq 0$, $m\omega_c t + n\omega_0 t$ is a carrier multiple of the side-band harmonics.

For the inverters with the N output level, the carrier vertical phase shifting SPWM modulation strategy requires $N - 1$ carrier, $N' = (N - 1)/2$ carriers in positive and negative half-circles, 1 peak of the triangular carrier, 1 modulation wave, modulation degree, and the smallest integer greater than $N' M$ to be set. According to the above bilateral Fourier transformation theory, the harmonic analysis expression for APOD is as follows:

$$F(x, y) = N' + \sum_{n=1}^{\infty} [A_{0n} \cos n\omega_0 t + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} [A_{mn-APOD} \cos[n\omega_c t + (2n - 1)\omega_0 t]] \quad (9)$$

where, $y_0 = \frac{\pi}{2}$, $y_{(N'M)} = y_{N'} = ar \cos(\frac{1}{M})$, A_{0n} , $A_{mn-APOD}$ is

$$A_{0n} \begin{cases} N'M - \frac{N'M}{\pi} \sin 2y_{N'} - \frac{2N'M}{(n-1)\pi} \sin(n-1)y_{N'} \cdots n = 1 \\ \frac{4N'}{n\pi} \sin ny_{N'} - \frac{2N'M}{(n+1)\pi} \sin(n+1)y_{N'} - \frac{2N'M}{(n-1)\pi} \sin(n-1)y_{N'} \cdots n = 3, 5 \cdots \infty \\ 0 \cdots n = 2, 4 \cdots \infty \end{cases}$$

$$A_{mn-APOD} = \frac{2}{m\pi^2} \left\{ \sin\left(n\frac{\pi}{2}\right) J_n(m\pi N'M) \left[\frac{1}{n} \left(\sin 2ny_0 - \sin 2ny_{(N'M)} \right) + y_0 - y_{(N'M)} \right] \right\} - 2 \sum_{k=1, k \neq |n|}^{\infty} \sin\left(k\frac{\pi}{2}\right) J_k(m\pi N'M) \left[\frac{\sin(n+k)y_{(N'M)}}{n+k} + \frac{\sin(n-k)y_{(N'M)}}{n-k} \right]$$

When $\langle N'M \rangle \leq N$, the harmonic resolution expression of APOD is as follows:

$$F(x, y) = \langle N'M \rangle + N'M \cos \omega_0 t + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} A_{mn-APOD} \cos[m\omega_c t + (2n - 1)\omega_0 t]$$

where $A_{mn-APOD}$ is

$$A_{mn-APOD} = \frac{2}{m\pi} J_{2n-1}(m\pi N'M) \sin\left[(2n - 1)\frac{\pi}{2}\right] \cos[m\omega_c t + (2n - 1)\omega_0 t]$$

The formula shows that when working at $\langle N'M \rangle \leq N$, the output voltage of the inverter does not have carrier harmonics and carrier multiples, only side-band harmonics of carrier multiples [30]. When working at $\langle N'M \rangle > N$, the harmonic content increases the odd times of the base wave, while the other harmonic content is the same as the linear modulation region; only the amplitude is different. It is also known from the formula that the equivalent frequency does not increase with the increase in N but remains f_c ; the output harmonic amplitude decreases with the rise in the number of levels.

POD modulation strategy output voltage harmonic expression is as follows:

When

$$\langle N'M \rangle \leq N$$

$$F(x, y) = \langle N'M \rangle + N'M \cos \omega_0 t + \sum_{m=2C}^{\infty} \sum_{n=2C+1}^{\infty} A_{mn-POD_1} \cos[m\omega_c t + n\omega_0 t] + \sum_{m=2C+1}^{\infty} \sum_{n=2C+1}^{\infty} A_{mn-POD_2} \cos[m\omega_c t + n\omega_0 t] \quad (10)$$

When

$$\langle N'M \rangle > N$$

$$F(x, y) = N' + \sum_{n=1}^{\infty} A_{0n} \cos n\omega_0 t + \sum_{m=2C}^{\infty} \sum_{n=2C+1}^{\infty} A_{mn-POD_1} \cos[n\omega_c t + n\omega_0 t] + \sum_{m=2C+1}^{\infty} \sum_{n=2C+1}^{\infty} A_{mn-POD_1} \cos[n\omega_c t + n\omega_0 t] \quad (11)$$

From these formulas, it can be seen that the harmonic characteristics of the POD modulation voltage are the same as that of the APOD modulation output when working at $\langle N'M \rangle < N$. When working in $\langle N'M \rangle > N$, the odd harmonic of the base wave is increased. The equivalent carrier frequency is still f_c and has not been improved [31].

4. Results and Discussions

4.1. Simulation Model

A multi-level inverter simulation was successfully built using MATLAB 2017b and eight IGBT switches were used in the MLI—the 72 V and 144 V input D.C. voltage sources, respectively. The remaining four IGBT switches are connected to the R.L. load side, which acts as a polarity generator in the MLI, and the remaining four IGBT switches are connected

4.1. Simulation Model

A multi-level inverter simulation was successfully built using MATLAB 2017b and eight IGBT switches were used in the MLI—the 72 V and 144 V input D.C. voltage source respectively. The remaining four IGBT switches are connected to the R.L. load side, which acts as a polarity generator in the MLI, and the remaining four IGBT switches are connected to a D.C. voltage source, which serves as a voltage level generator. To obtain the necessary output voltage level at the multi-level inverter's output, PWM techniques are used. Phase opposition disposition (POD), alternative phase opposition disposition (APOD), and PWM with multiple carriers. A voltage waveform with seven levels is produced via multi-carrier PWM. The FFT tool in MATLAB 2017b can be used to calculate the total harmonic distortion (THD). The logical circuit side of the simulation model's OR, XOR, NXOR, and NOT gates regulate the switching operation (ON and OFF) in the CHB-MLI, as illustrated in Figure 11. The specification of the parameters is given in Table 5. The specification of the parameters is given in Table 5.

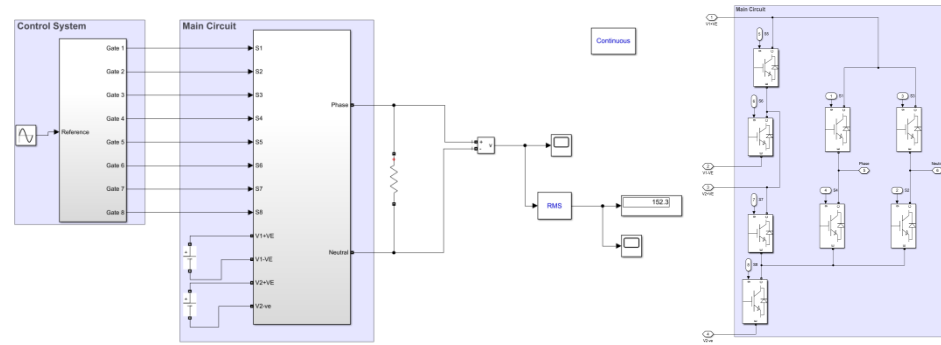


Figure 11. Simulation Model of CHB-MLI.

Table 5. The specification of the parameters used in the simulation model.

Parameter	Parameter	Specification	Specification
The input voltage	The input voltage	72 and 144 V	72 and 144 V
Output voltage level	Output voltage level	7	7
Switch	Switch	IGBT	IGBT
Without a switch:	Without a switch:	8	8
R.L. load	R.L. load	100 ohms, 2×10^{-3} H	100 ohms, 2×10^{-3} H

For the control circuit, seven repeating sequences are used and compared with the sinusoidal waveform, which can be seen and analyzed with the help of scope; that seven relational operations are used, which are connected with the seven repeating sequences and logical gates (XOR and NXOR); the logical gates are sent signals through switching gates, which turn the IGBT ON and OFF. The control circuit of simulation model is shown in Figure 12. The export of CHB-MLI. The Control Circuit of Simulation Model is shown in Figure 12.

4.2. Simulation Results

In this section, we present the simulation results. After obtaining the harmonic analytical expression of the above multi-level modulation strategy, taking APOD and POD modulation strategy as an example, MATLAB was used for simulation to verify the harmonic characteristics indicated by the analytical expression.

4.2.1. APOD MC PWM Modulation Strategy

In this section, we present the simulation of the inverter of the APOD modulation strategy. The diagram of the simulation is shown in Figure 11. When the high voltage D.C. bus voltage is set at 144 V and the low voltage D.C. bus voltage is set at 72 V, then the output voltage levels are 216 V, 144 V, 72 V, 0 V, -72 V, -144 V, -216 V.

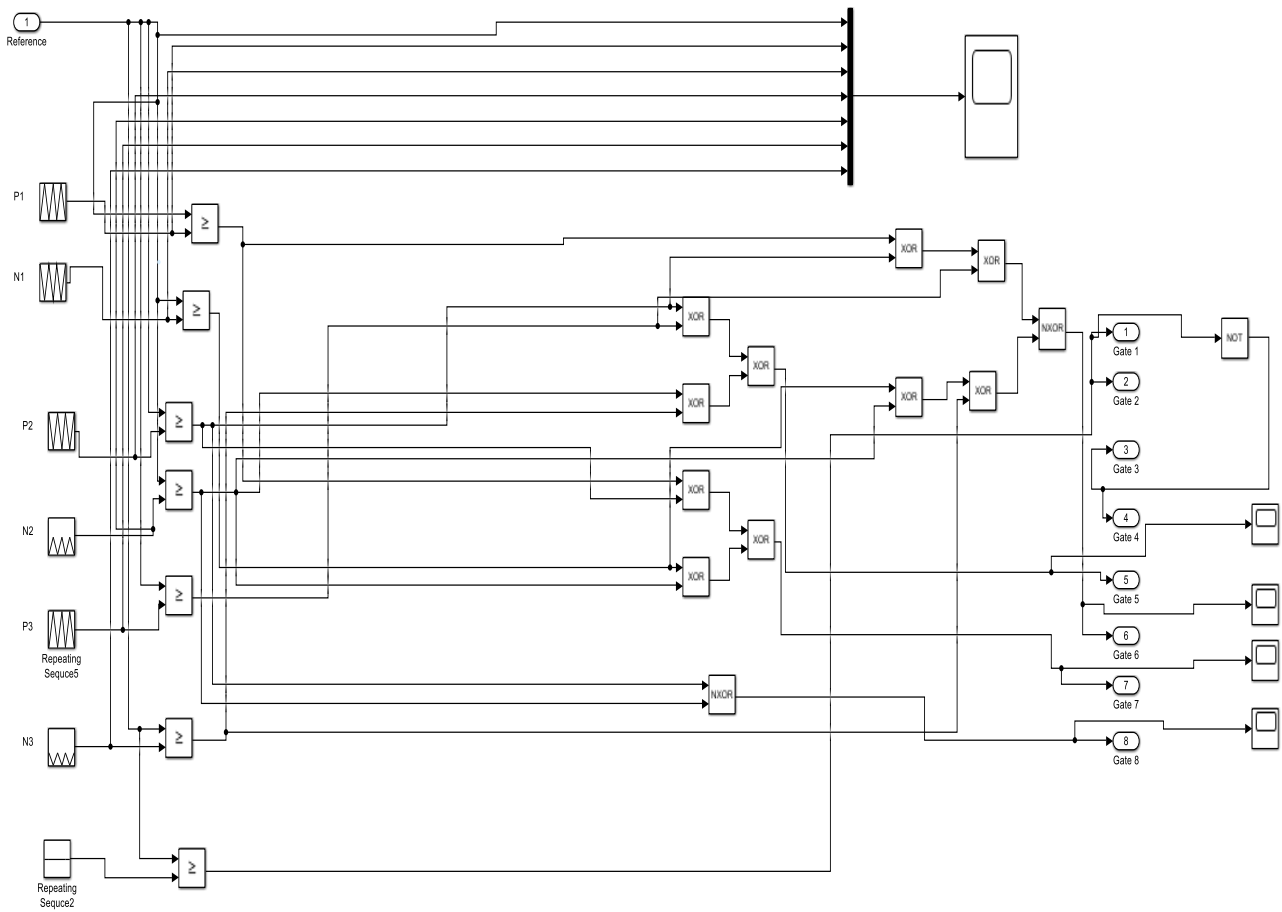


Figure 12. Control Circuit of Simulation Model.

The APOD modulation strategy was adopted for the inverter modulation strategy, and the carrier frequency was set at 1 kHz, 5 kHz, and 10 kHz, respectively. The carrier and modulation waveforms with the carrier frequency set at 1 kHz are shown in Figure 13 and Figure 14, respectively. In this section, we present the simulation results. After obtaining the harmonic voltage expression of the above multi-level modulation strategy, taking APOD and POC modulation strategy as an example, MATLAB was used for simulation to verify the harmonic characteristics indicated by the analytical expression.

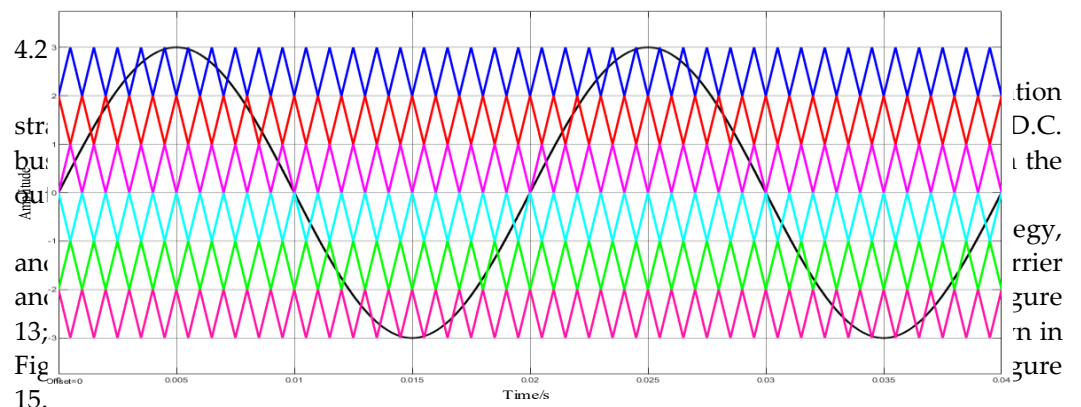
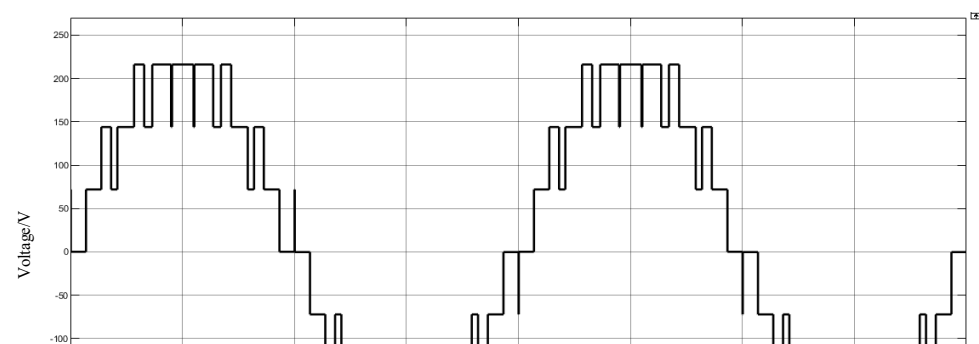


Figure 13. Carrier and modulation of APOD MC PWM waveform with 1 kHz frequency.



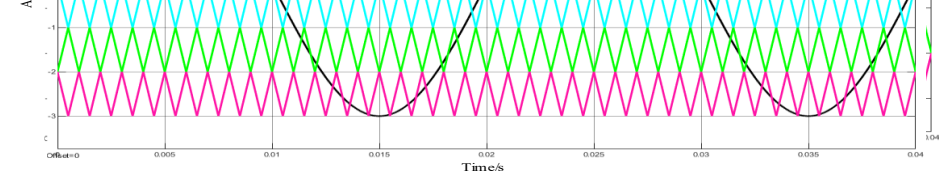


Figure 13. Carrier and modulation of APQD MC PWM waveform with 1 kHz frequency.

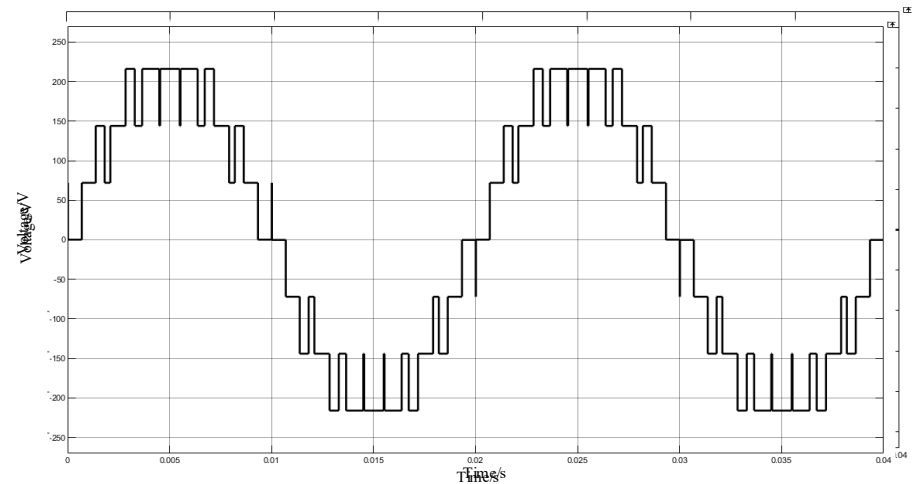


Figure 14. Voltage waveform of APQD MC PWM with 1 kHz frequency.

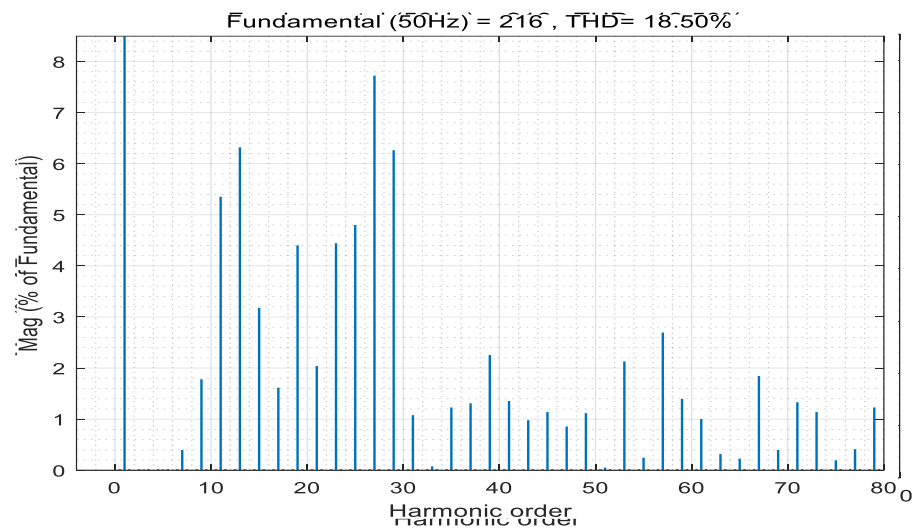


Figure 15. Total harmonic distortion of APQD MC PWM with 1 kHz frequency.

The carrier and modulation waveforms with the carrier frequency set at 5 kHz and 1 Hz are shown in Figure 16; the voltage simulation waveform with the carrier frequency set at 5 kHz is shown in Figure 17; and the THD analysis with the carrier frequency set at 5 kHz is shown in Figure 18.

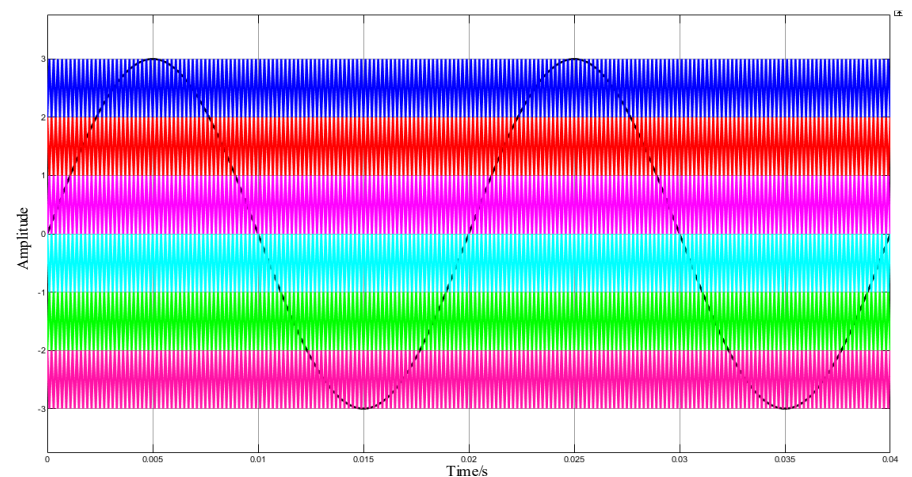
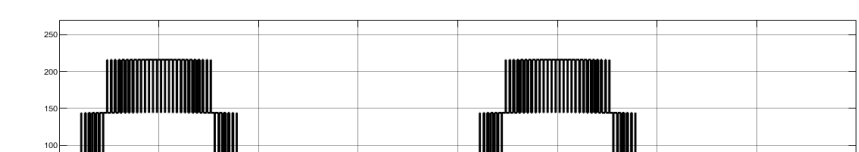


Figure 16. Carrier and modulation of APQD MC PWM waveform with 5 kHz frequency.



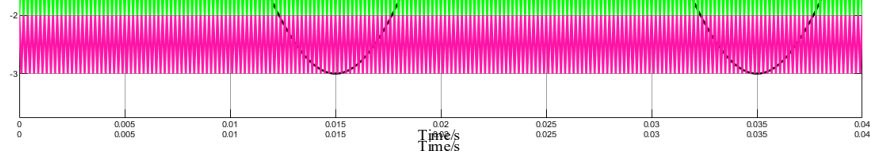


Figure 16: Carrier and modulation of APOD MC PWM waveform with 5 kHz frequency.

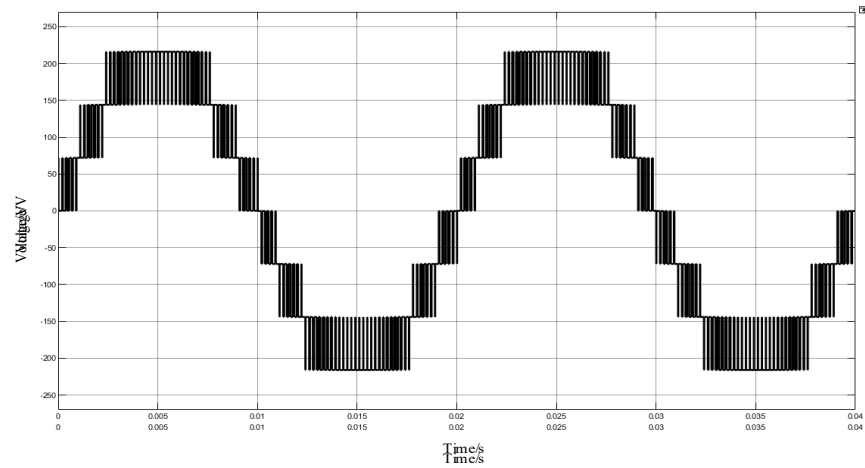


Figure 17: Voltage waveform of APOD MC PWM with 5 kHz frequency.

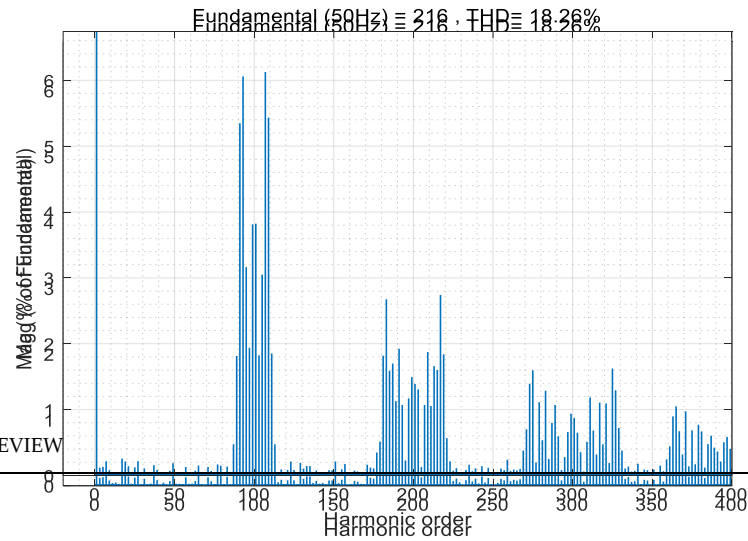


Figure 18: Total harmonic distortion of APOD MC PWM with 5 kHz frequency.

The carrier and modulation wave waveforms with the carrier frequency, set at 10 kHz are shown in Figure 19; the voltage simulation waveform with the carrier frequency set at 10 kHz is shown in Figure 20, and the THD analysis with the carrier frequency set at 10 kHz is shown in Figure 21.

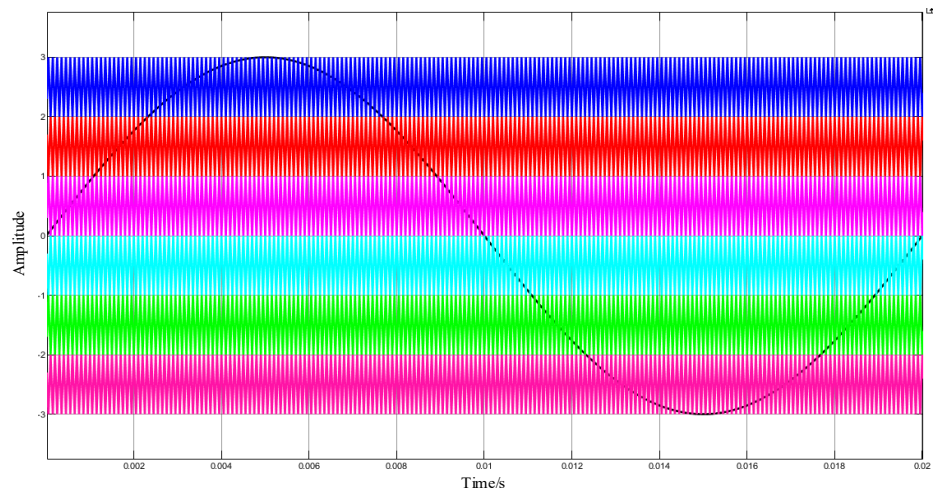
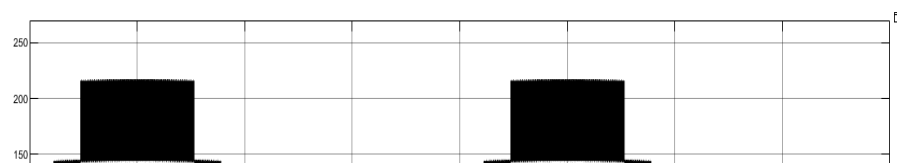


Figure 19: Carrier and modulation of APOD MC PWM waveform with 10 kHz frequency.



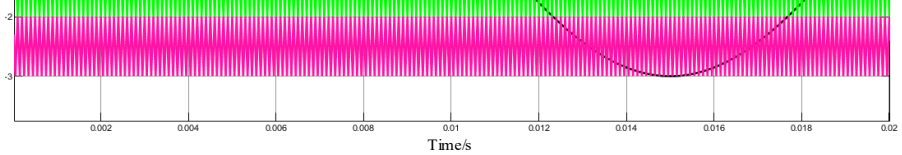


Figure 19. Carrier and modulation of APOD MC PWM waveform with 10 kHz frequency.

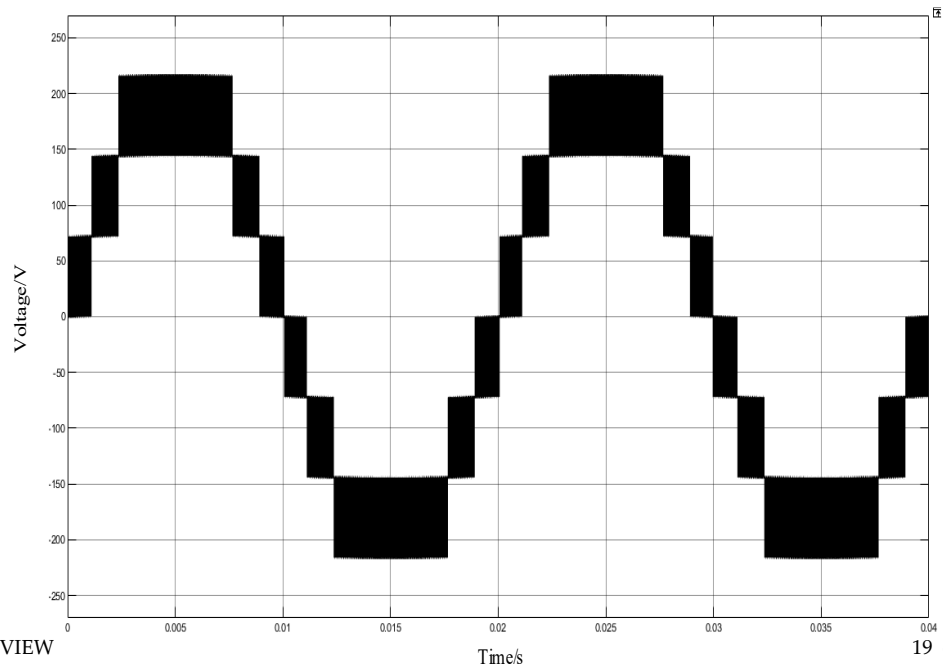


Figure 20. Voltage waveform of APOD MC PWM with 10 kHz frequency.

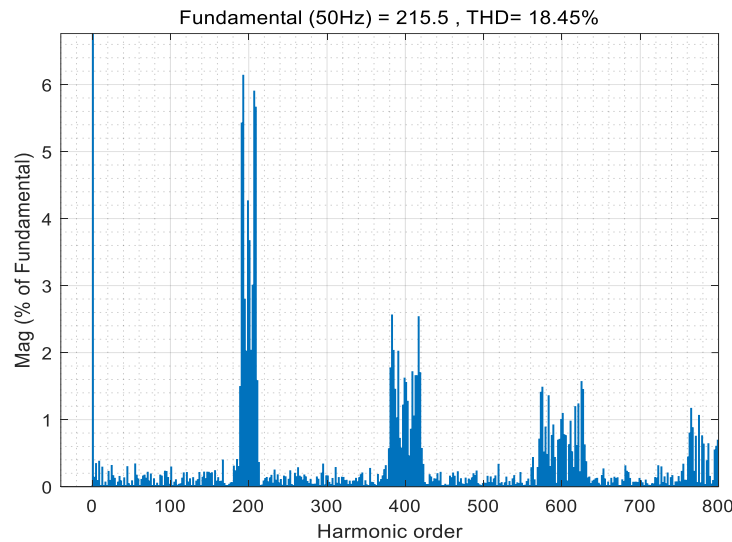
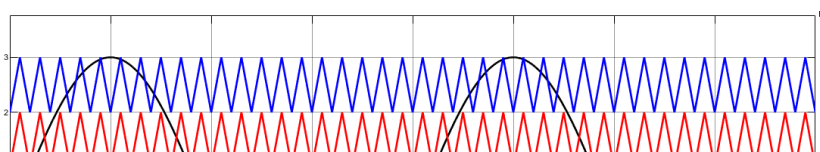


Figure 21. Total harmonic distortion of APOD MC PWM with 10 kHz frequency.

It can be seen from Figures 15, 18 and 21 that the most severe harmonic caused by the APOD modulation strategy is located at the primary carrier frequency f_c , and more harmonic energy is injected into the carrier harmonic. There are carrier harmonics and carrier multiple side-band harmonics in the spectrum, and the average switching frequency of the switch device is equal to the carrier frequency. This is relevant to the theoretical analysis results of Formula (10) and (11). At the same time, from the simulation results, simply changing the modulation frequency has little effect on the THD.

4.2.2. POD MC PWM Modulation Strategy

The POD modulation strategy was adopted for the inverter modulation strategy, and the carrier frequency was set at 1 kHz, 5 kHz, and 10 kHz, respectively. The carrier and modulation waveforms with the carrier frequency set at 1 kHz are shown in Figure 22; the voltage simulation waveform with the carrier frequency set at 1 kHz is shown in Figure 23; and the THD analysis with the carrier frequency set at 1 kHz is shown in Figure 24.



The POD modulation strategy was adopted for the inverter modulation strategy, and the carrier frequency was set at 1 kHz, 5 kHz, and 10 kHz, respectively. The carrier and modulation waveforms with the carrier frequency set at 1 kHz are shown in Figure 22; the voltage simulation waveform with the carrier frequency set at 1 kHz is shown in Figure 23; and the THD analysis with the carrier frequency set at 1 kHz is shown in Figure 24.

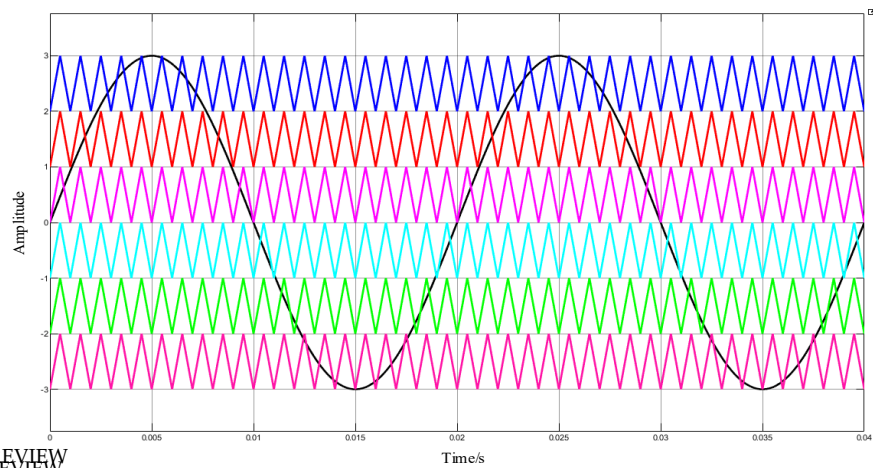


Figure 22. Carrier and modulation waveform of POD MC PWM with 1 kHz frequency.

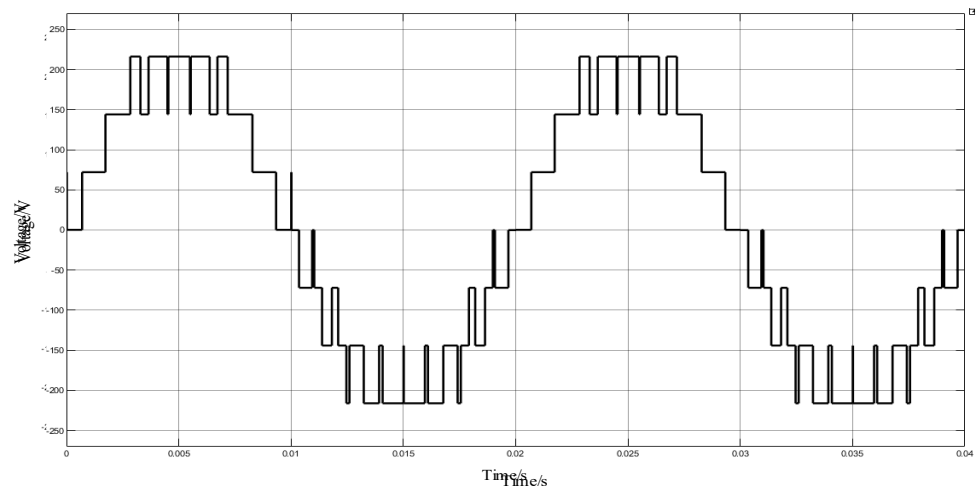


Figure 23. Voltage waveform of POD MC PWM with 1 kHz frequency.

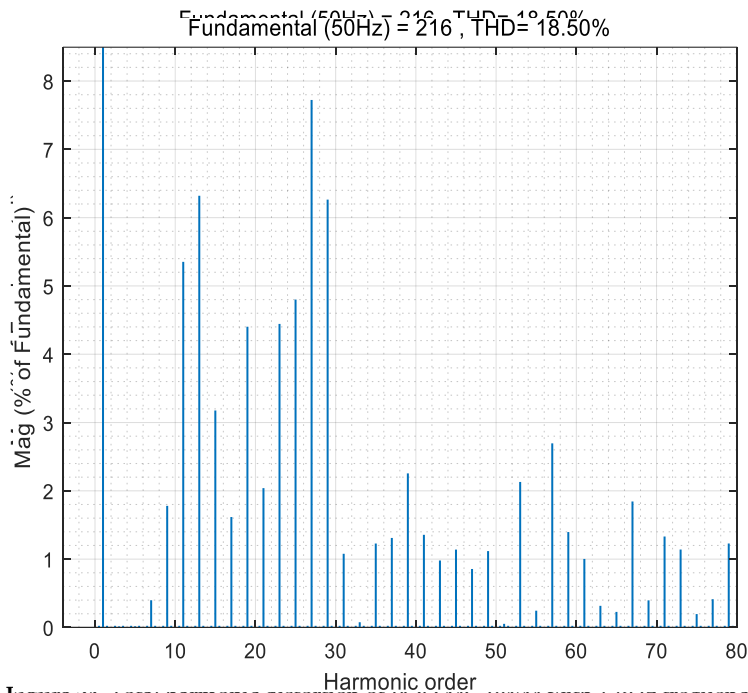


Figure 24. Total harmonic distortion of POD MC PWM with 1 kHz frequency.

Figure 24. Total harmonic distortion of POD MC PWM with 1 kHz frequency.

The carrier and modulation waveforms with the carrier frequency set at 5 kHz are shown in Figure 25 and the voltage simulation waveform with the carrier frequency set at 5 kHz is shown in Figure 26 and the THD analysis with the carrier frequency set at 5 kHz is shown in Figure 26; and the THD analysis with the carrier frequency set at 5 kHz is shown in Figure 27.

The carrier and modulation wave waveforms with the carrier frequency set at 5 kHz are shown in Figure 25; the voltage simulation waveform with the carrier frequency set at 5 kHz is shown in Figure 26; and the THD analysis with the carrier frequency set at 5 kHz is shown in Figure 27.

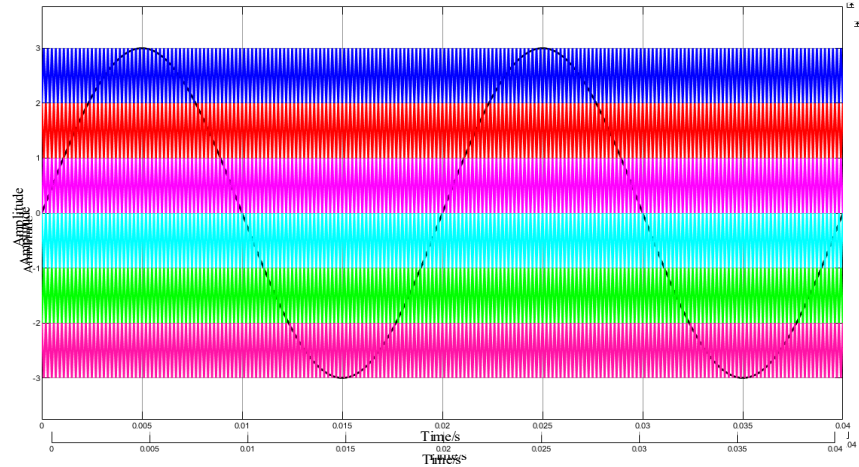


Figure 25. Carrier and modulation waveforms of POD MC PWM with 5 kHz frequency.

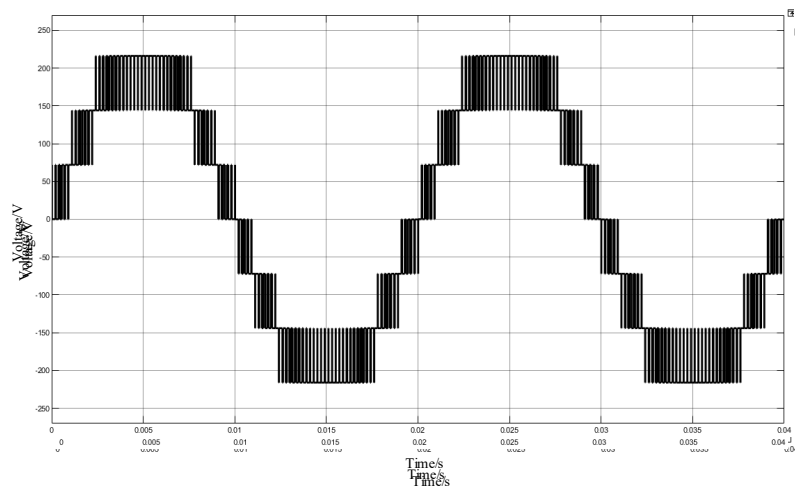


Figure 26. Voltage waveform of POD MC PWM with 5 kHz frequency.

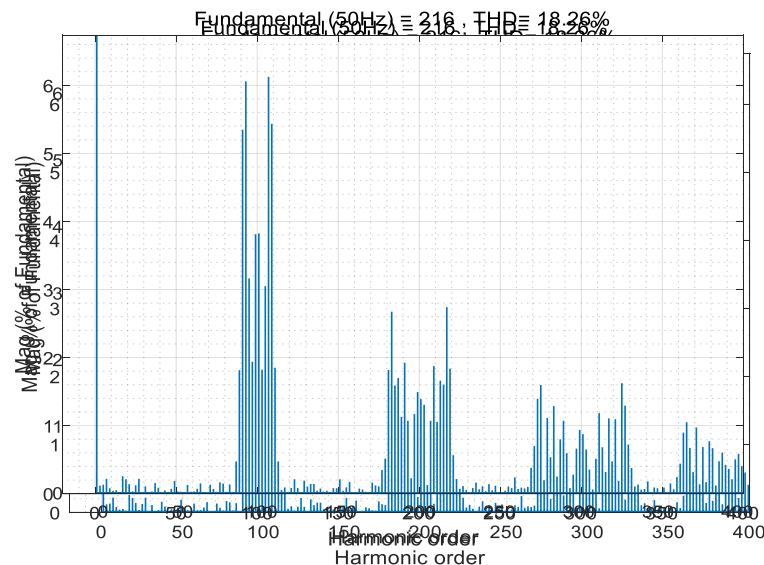


Figure 27. Total harmonic distortion of POD MC PWM with 5 kHz frequency.

The carrier and modulation waveforms with the carrier frequency set at 10 kHz are shown in Figure 28; the voltage simulation waveform with the carrier frequency set at 10 kHz is shown in Figure 29; and the THD analysis with the carrier frequency set at 10 kHz is shown in Figure 30.

It can be seen from Figures 24, 27 and 30 that the most severe harmonic caused by the POD modulation strategy is located at the primary carrier frequency f_c , and more harmonic energy is injected into the carrier harmonic. There are carrier harmonics and carrier multiple side-band harmonics in the spectrum, and the average switching frequency of the switch device is equal to the carrier frequency. This is relevant to the theoretical analysis results of Formulas (10) and (11). At the same time, from the simulation results, simply changing the modulation frequency has little effect on the THD.

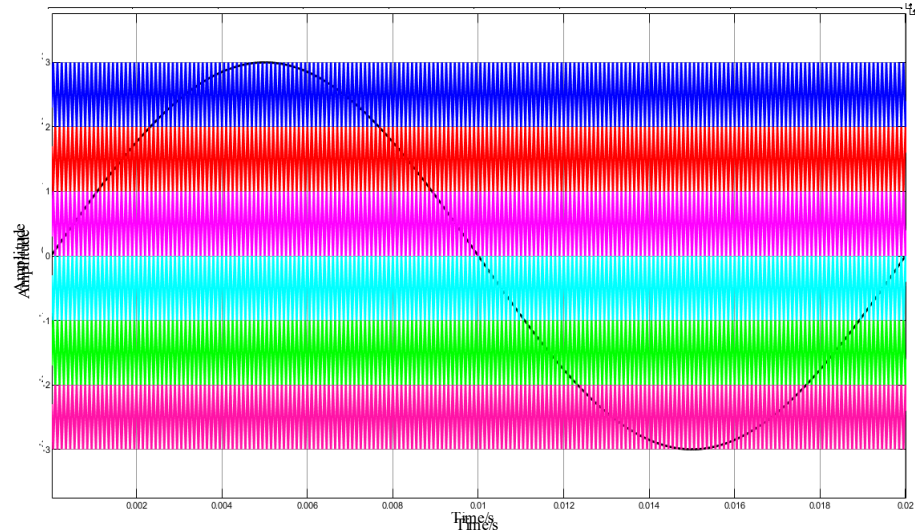


Figure 28. Carrier and modulation waveform of POD MC PWM with 10 kHz frequency.

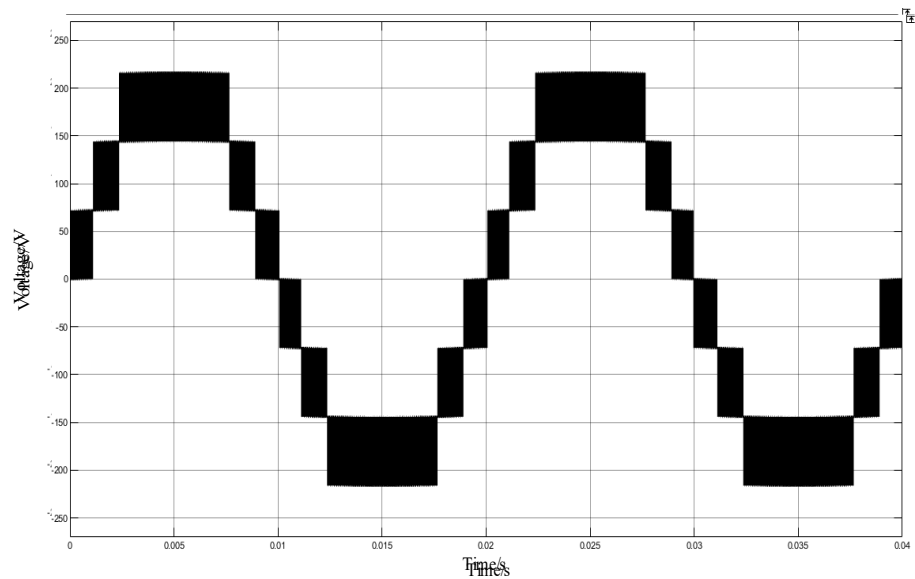


Figure 29. Voltage waveform of POD MC PWM with 10 kHz frequency.

It can be seen from Figures 24, 27 and 30 that the most severe harmonic caused by the POD modulation strategy is located at the primary carrier frequency f_c , and more harmonic energy is injected into the carrier harmonic. There are carrier harmonics and carrier multiple side-band harmonics in the spectrum, and the average switching frequency of the switch device is equal to the carrier frequency. This is relevant to the theoretical analysis results of Formulas (10) and (11). At the same time, from the simulation results, simply changing the modulation frequency has little effect on the THD.

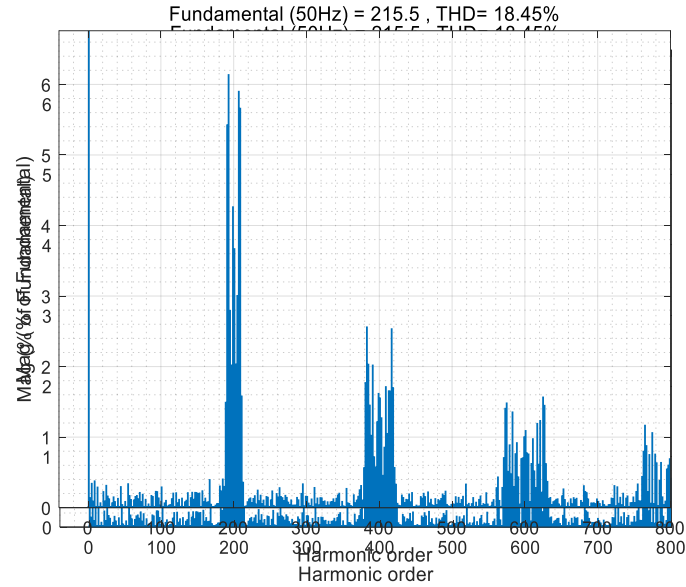


Figure 30. Total Harmonic Distortion of BOD MC PWM with 10 kHz frequency.
 Figure 30. Total Harmonic Distortion of BOD MC PWM with 10 kHz frequency.

4.2.3. Variable Carrier Frequency APOD Modulation Strategy

The variable carrier frequency SPWM modulation strategy can improve the equivalent carrier frequency and the APOD modulation strategy can significantly decrease the harmonic content of the output voltage. By combining the two, this paper proposes a variable carrier frequency APOD modulation strategy (VF-APOD).

The schematic diagram of the simulation structure is shown in Figure 11. When the high voltage D.C. bus voltage is set at 144 V and the low voltage D.C. bus voltage is set at 72 V, then the output voltage levels are 216 V, 144 V, 72 V, 0 V, -72 V, -144 V, -216 V. The variable carrier frequency VF-APOD modulation strategy is used in the inverter. The carrier frequencies are 1 kHz, 4 kHz, and 500 Hz, respectively. The carrier and modulation waveforms are shown in Figure 31; the voltage simulation waveform is shown in Figure 32; and the THD analysis is shown in Figure 33.

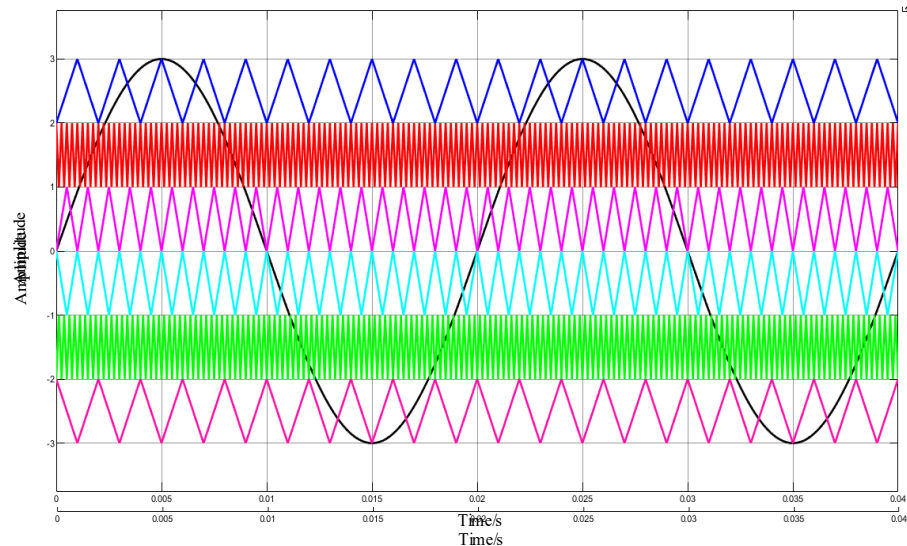


Figure 31. Carrier and modulation waveform of VF-APOD MC PWM.
 Figure 31. Carrier and modulation waveform of VF-APOD MC PWM.

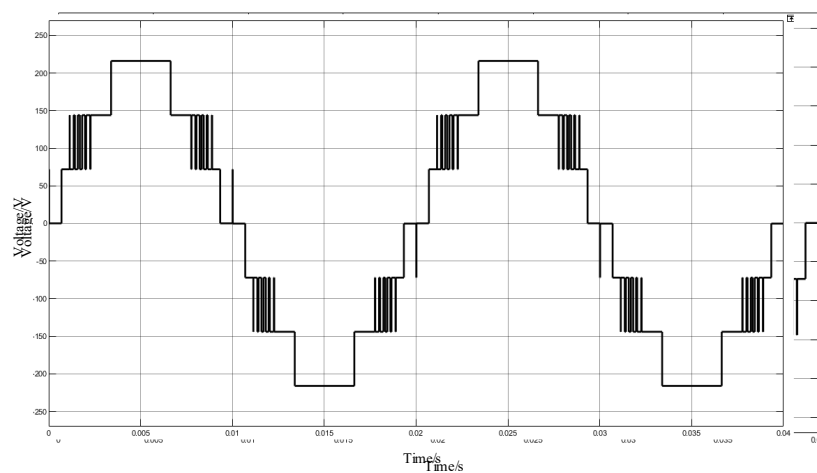


Figure 32. Voltage simulation waveform of VF-APOD MC PWM.

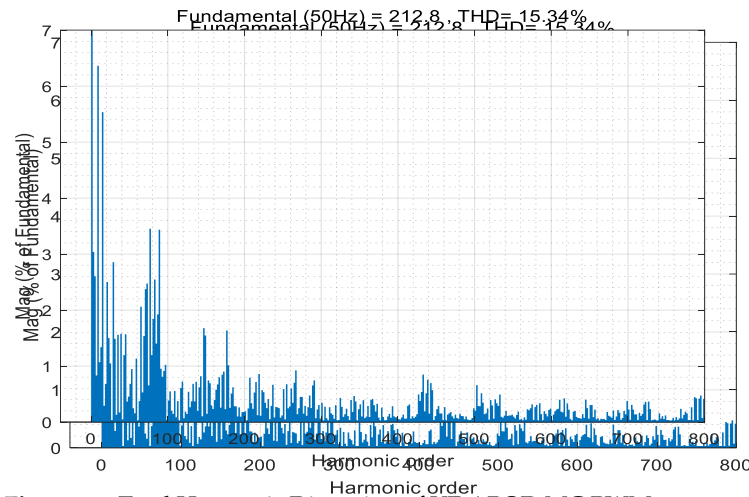


Figure 33. Total Harmonic Distortion of VF-APOD MC PWM.

The simulation results show that the THD has decreased significantly from 18% to 15.34%. As the carrier frequency increases with the OPD modulation strategy, the switching frequency of the VF-APOD modulation strategy is much lower. Theoretically, this modulation strategy can significantly reduce the switch's loss and performance requirements.

4.3. DSP Programming

4.3. DSP Programming

The experiment platform uses the In TI DSP 28335 as the controller; the control strategy is programmed in C language, and the control platform is shown in Figure 34. The C code of the control strategy is shown in Figure 35.

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Figure 34. DSP control platform.

```

void main(void)
{
    InitSysCtrl();
    DINT;
    IER = 0x0000;
    IFR = 0x0000;
    InitPieCtrl();
    InitPieVectTable();
    InitGpio();
    InitXintf();
    InitCpm();
    InitAdc();
    PieCtrlRegs.PIEIER1.bit.INTx1 = 1; //Enable PIE_SEQ1_INT

    EPwm2Regs.TBCTL.bit.HSPCLKDIV = 1; //MSPCLK=150/2=750Hz
    EPwm2Regs.TBCTL.bit.CLKDIV = 1; //TBCLK=750/20=37.5kHz
    EPwm2Regs.TBCTL.bit.FREE_SOFT = 1; //Stop when TBCTR = 0x0000
    EPwm2Regs.TBCTL.bit.PRSVDIV = 1; //Count up after the synchronization event
    EPwm2Regs.TBCTL.bit.SYNCOSL = 3; //Disable EPWM2SYNCO signal
    EPwm2Regs.TBCTL.bit.PBOLD = 0; //Shadow register
    EPwm2Regs.TBCTL.bit.PWSEN = 0; //Do not load the TBCTR from the TBPMS
    EPwm2Regs.TBCTL.bit.CTRMODE = 2; //Up-down mode
    EPwm2Regs.TBSTS.bit.CTRRST = 1; //Clear main value flag
    EPwm2Regs.TBSTS.bit.SVNC1 = 1; //Clear external synchronization event flag

    EPwm2Regs.TBPRD = 0x493E; //Up-down mode Period = 1ms
    EPwm2Regs.TBCTR = 0; //CTR start from 0
    EPwm2Regs.TBMS.bit.TBPHS = 0; //TBPMS register is 0
    EPwm2Regs.CMPCTL.bit.SHDWNOVDE = 0; //Compare A register shadow mode
    EPwm2Regs.CMPCTL.bit.LOADMODE = 0; //Compare A register load on when CTR=0x0000
    
```



Figure 34. DSP control platform.

```

void main(void)
{
    InitSysCtrl();
    DINT;
    IER = 0x0000;
    IFR = 0x0000;
    InitPieCtrl();
    InitPieVectTable();
    InitPie();
    InitXintf();
    InitEPwm();
    InitAdc();
    PieCtrlRegs.PIEIER1.bit.INTx1 = 1; //Enable PIE SEQ1_INT
    PieCtrlRegs.PIEIER2.bit.INTx1 = 1; //Enable PIE EPMW1_TZINT
    IER |= INT1; //Enable CPU interrupt 1
    IER |= INT2; //Enable CPU interrupt 2
    EINT;
    ERTH; //Enable debug
    EALLOW;
    SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1; //Start EPMW1 clock, globally synchronize
    EDIS;
    Sys_Start();
}

//-----EPWM0-----
EpmwRegs.TBCTL.bit.HSPCLKDIV = 1; //HSPCLK=150/2=75MHz
EpmwRegs.TBCTL.bit.CADIV = 1; //TBCLK=75/2=37.5MHz
EpmwRegs.TBCTL.bit.FREE_SOFT = 1; //Stop when TBCTR = 0x0000
EpmwRegs.TBCTL.bit.PRODIR = 1; //Count up after the synchronization event
EpmwRegs.TBCTL.bit.SWGSEL = 3; //Disable EPWM0SYNC signal
EpmwRegs.TBCTL.bit.PRSSEL = 0; //Shadow register
EpmwRegs.TBCTL.bit.PRSIN = 0; //Do not load the TBCTR from the TBPMS
EpmwRegs.TBCTL.bit.CTRMODE = 2; //Up-down mode
EpmwRegs.TBSTS.bit.CTRMAX = 1; //Clear max value flag
EpmwRegs.TBSTS.bit.SINCE = 1; //Clear external synchronization event flag

EpmwRegs.TBPRD = 0x003E; //Up-down mode period = 1ms
EpmwRegs.TBCTR = 0; //CTR start from 0
EpmwRegs.TBPHS.half_TBPHS = 0; //TBPHS register is 0
EpmwRegs.CMPCTL.bit.SHDWMODE = 0; //Compare A register shadow mode
EpmwRegs.CMPCTL.bit.LOADMODE = 0; //Compare A register load on when CTR=0x0000
EpmwRegs.CMPA.half_CMPA = 0; //Init compare A register

EpmwRegs.AQCTLA.bit.CAU = 1;
EpmwRegs.AQCTLA.bit.CAD = 2;
EpmwRegs.AQCTLB.bit.CAU = 1;
EpmwRegs.AQCTLB.bit.CAD = 2;
EpmwRegs.AQFRC.bit.ALDLDF = 0; //Shadow mode, load an event when CTR=0

EpmwRegs.DRCTL.bit.IN_MODE = 2; //AQ EPWMA rising-edge delay; EPWMB falling-edge delay
EpmwRegs.DRCTL.bit.INVLSL = 2; //EPWMB inverted
EpmwRegs.DRCTL.bit.OUT_MODE = 3; //Enable rising and falling delay
EpmwRegs.DDRED = 0x0000; //Rising delay bus
EpmwRegs.DDFED = 0x0000; //Falling delay bus

EpmwRegs.TISEL.bit.OSM1T = 1; //Enable TZ1 as a one-shot trip source for EPW2 (Over Current Protect)
EpmwRegs.TZCTL.bit.TZA = 2; //Force EPWMA to a low state
EpmwRegs.TZCTL.bit.TZB = 2; //Force EPWMB to a low state
EpmwRegs.TZCLR.bit.CST = 1; //Clear flag for one-shot trip latch
    
```

Figure 35. Code of DSP programming.

4.4. Real-Time Simulation Testing in Xsim System

To test the control function, the primary seven-level converter model is built up in the Xsim real-time simulation system. The Xsim system provides a rapid development platform from simulation to prototype and realizes the application of the simulation model in product development, simulation verification, and on-site debugging. By parallelizing and optimizing simulation technology, the Xsim system can realize the optimization of real-time simulation.

The simulation monitoring software is shown in Figure 36. The simulation data can be monitored, the code can be automatically generated and downloaded, the simulation process can be monitored, the results can be displayed, and the parameters can be adjusted online. The parallel computation of the simulation model and a real-time storage of simulation data are realized. In addition, the real-time simulator with the I/O interface board card is used to complete the analog and digital signal high-speed acquisition and output, as well as the real-time simulator and other equipment clock synchronization and data communication.

The carrier waveform and modulation based on APOD from the Xsim system are shown in Figure 37. The output voltage of the inverter from the Xsim system is shown in Figure 38.

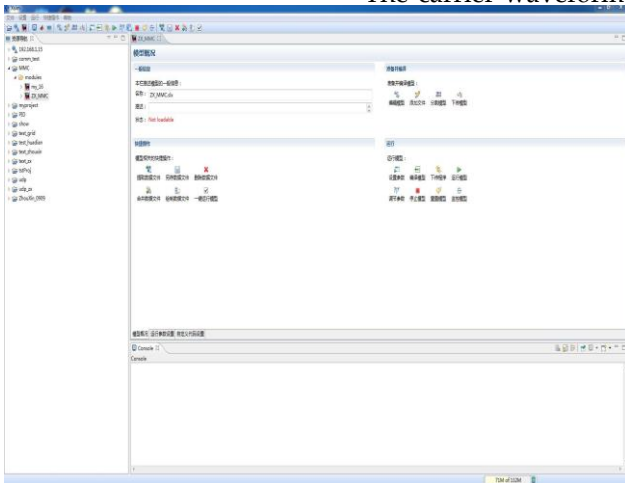


Figure 36. Real-time hardware and software simulations of the Xsim system.

The carrier waveform and modulation based on APOD from the Xsim system are shown in Figure 37. The output voltage of the inverter from the Xsim system is shown in Figure 38.

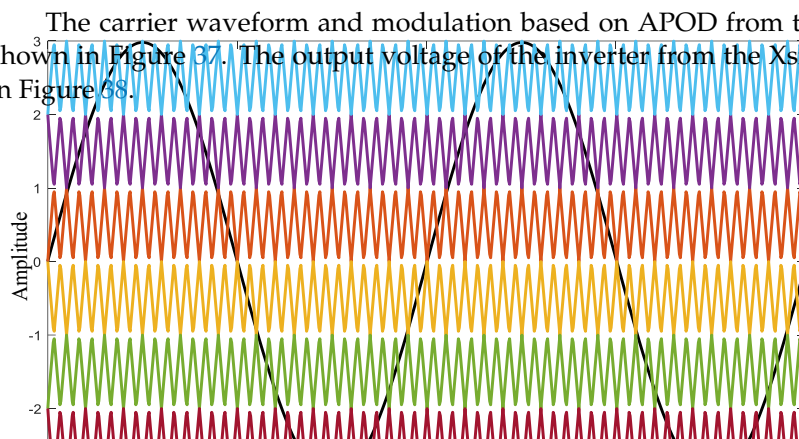




Figure 36. Real-time hardware and software simulations of the Xsim system.

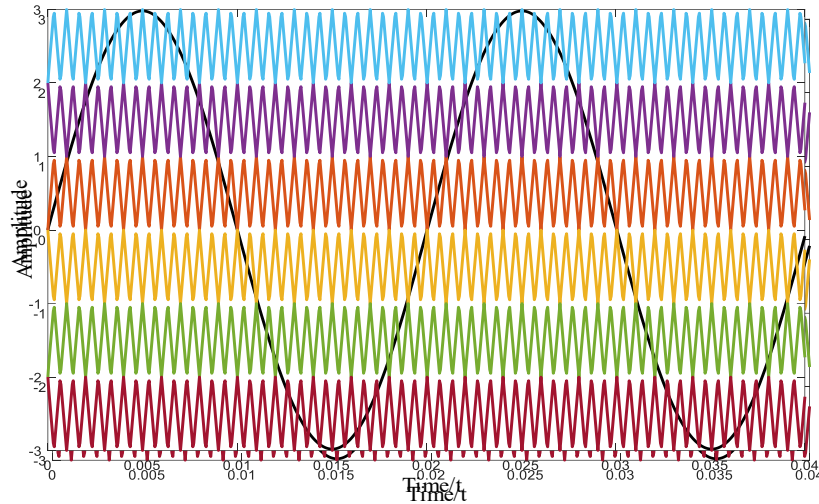


Figure 37. Carrier and modulation waveform from the Xsim system.

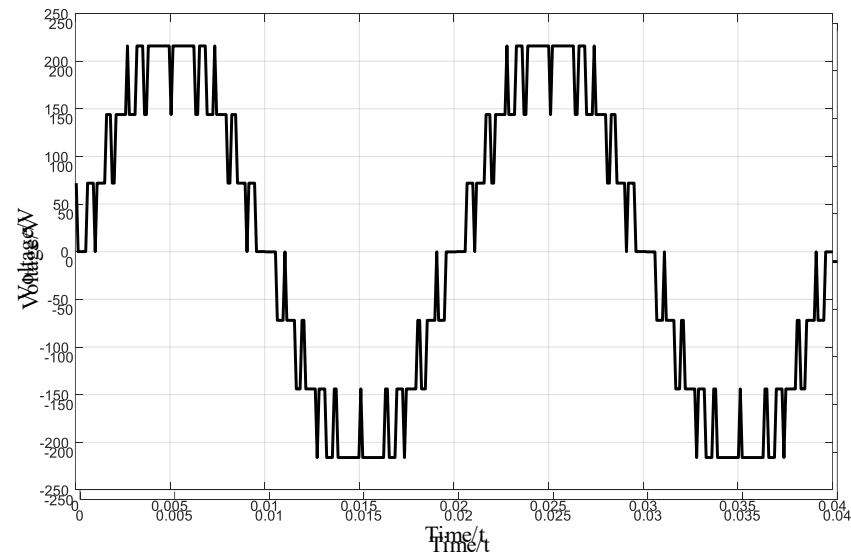


Figure 38. Waveform of output voltage from the Xsim system.

In the above discussion, the correctness of the theoretical analysis of the APOD and POD modulation strategy is verified by the simulation of a multi-level converter at different frequencies, and a VF-APOD modulation strategy is proposed and simulated based on it, which verifies the advantage of the variable carrier VF-APOD in reducing the THD.

5. Conclusions

MATLAB successfully implemented the multi-level inverter model to generate a seven-level output voltage waveform for the CHB MLI. Two modulation techniques, APOD (alternate phase opposition disposition) MC PWM and POD (phase opposition disposition) MC PWM, were used to obtain the desired output voltage waveform. The THD (total harmonic distortion) was determined and analyzed using the FFT tool in MATLAB. The APOD technique achieved an output voltage THD of 18.27%, while the APOD PWM technique achieved an output current THD of 15.67%. On the other hand, the POD PWM technique achieved an output voltage THD of 18.06% and an output current THD of 15.45%. The results have established that the POD multi-carrier PWM produces more precise output voltage and current waveforms compared to the APOD multi-carrier pulse width modulation (PWM).

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